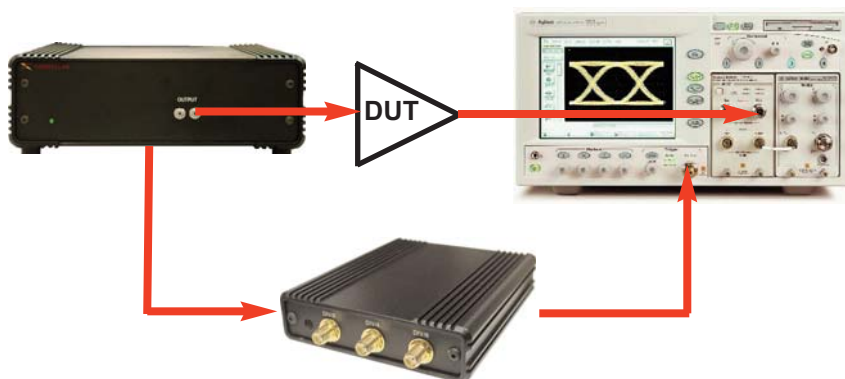


11 - 21Gb/s PRBS SOURCE



Features

- High Performance PRBS Generator
- 11 to 21 Gb/s data rates
- 2e7, 2e15, and 2e31 patterns
- 800 mV differential output
- External clock input
- Ultra-low jitter, 400 fs rms
- Centellax Divider module for low frequency trigger inputs.
- Pattern trigger output
- Centellax Driver Amplifiers optional for higher output swing (>3V or >7V)
- Small size (7" x 10" x 2.5")

Driver Amplifier Test Set-up

Shown above is a typical measurement setup for measuring modulator driver amplifiers. Included is a divide by 8 (TD40MCA) for scope triggering.

Description

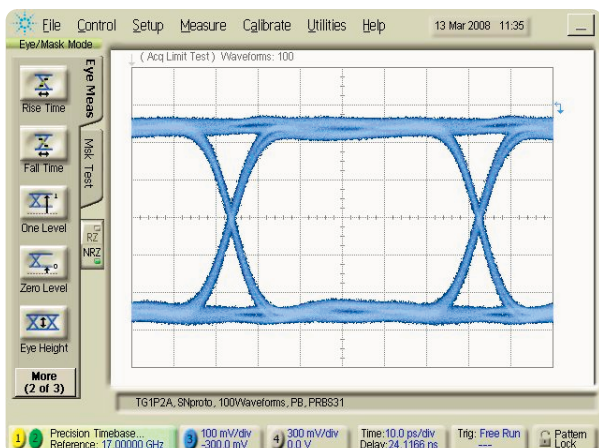
The Centellax TG1P2A Source is an 11-21 Gbps PRBS generator. This product has been designed to provide an excellent quality "EYE" at a fraction of the price of current market solutions. This is made possible through comprehensive integration of the key building blocks into monolithic integrated circuits founded on SiGe technology. The performance of the 11-21 Gbps PRBS Source is world class with the typical EYE having 400 fs rms jitter, 400 mV of output swing and <7 ps rise time. All of this comes in a package one sixth the size of any other solution on the market which allows you to put your source directly at your device under test regardless of your lab bench environment.

Application

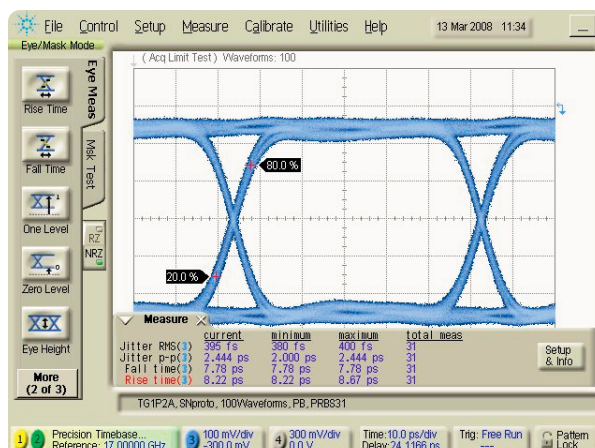
The Centellax 11-21 Gbps PRBS Source is designed to be used as the source for testing high speed communications components, such as those used in fiber channel applications. The 11-21 Gbps PRBS Source is a perfect companion to a Digital Communication Analyzer in a stimulus response measurement for 11-21 Gbps components. Other applications include backplane signal integrity testing, and cable testing.

Note: Outputs are CML and must be externally DC terminated with 50Ω to GND. One way to achieve DC termination while AC coupling is to use a Bias-Tee with its DC pin grounded.

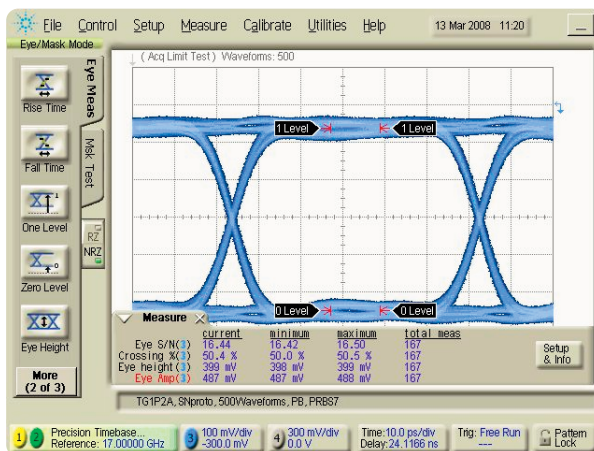
TG1P2A Datasheet



17 Gb/s



17 Gb/s



17 Gb/s

Label	Description		
Power	Power Switch on/off		
Clk Input	External Clock Input (11 - 21GHz)		
Clk / 1	'Clk Input' Output		
Reset	Reset / PRBS Pattern		
Pattern Trigger	Pattern Trigger Output		
Pattern Length	Pattern Selector		
	Logic	Pattern	Polynomial Description
	1 1	$2^{31} - 1$	$1 + x^{28} + x^{31}$
	1 0	$2^{15} - 1$	$1 + x^{14} + x^{15}$
0 0	$2^7 - 1$	$1 + x^4 + x^7$	

Performance Specification Table

	Description	Minimum	Typical	Maximum	Unit
DATA OUTPUT	Bit Rate TG1P2A	11	-	21	Gb/s
	RMS Jitter TG1P2A	-	400	600	fs
	Rise/Fall Times (20-80%)	-	7.0	8	ps
	Amplitude	450	480	-	mVpp
	SNR	-	16	-	
	Crossing	50	55	60	%
	Output Level High Low	-50 -450	0 -	- -600	mV mV
CLOCK INPUT	Input Level	8	-	12	dBm
	Offset	-	0	-	V
	Frequency	11	-	21	GHz
PATTERN TRIGGER OUTPUT	Output Level	-	500	-	mV
	Jitter	-	20	-	ps
CLK/I OUTPUT	Output Level (Input = +10dBm)	-4	-	-2	dBm
PHASE ADJUSTMENT	Phase adjustment range	-	30	-	ps
PATTERN TRIGGER	Pulse Rate:	$64 * (1/\text{Output_Bit_Rate}) * (2^n - 1)$			
	Pulse Width:	$64 * (1/\text{Output_Bit_Rate})$			