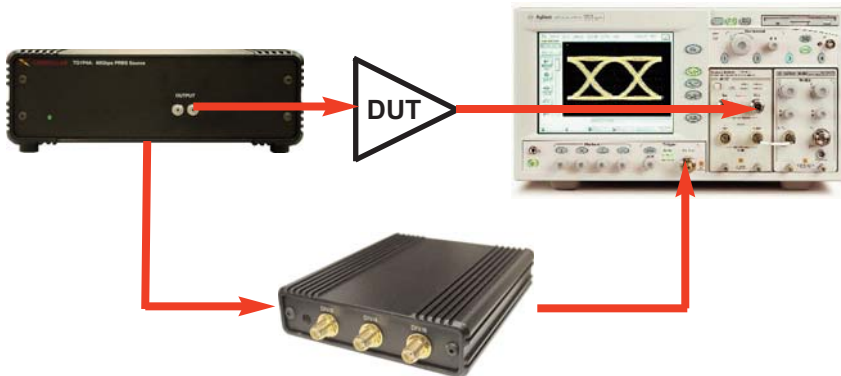


22 - 44Gb/s PRBS SOURCE

Features

- Self-contained PRBS Generator
- 22 to 44 Gb/s data rates
- Built-in oscillator (39.8 Gb/s)
- 2e7, 2e15, and 2e31 patterns
- 1000 mV differential output
- Ultra low noise trigger provided (20 GHz) for precision time base applications
- External clock input
- Ultra-low jitter, 400 fs rms
- Centellax Divider module for low frequency trigger inputs.
- Pattern trigger output
- Option for Internal Reference Clock for operation at 28.000 Gb/s.
- Centellax Driver Amplifiers optional for higher output swing (>3V or >7V)
- Small size (7" x 10" x 2.5")



Driver Amplifier Test Set-up

Shown above is a typical measurement setup for measuring modulator driver amplifiers. Included is a divide by 8 (TD40MCA) for scope triggering.

Description

The Centellax 22-44Gb/s PRBS Source is a fully self-contained 40 Gb/s pattern generator. This product has been designed to provide an excellent quality "EYE" at a fraction of the price of current market solutions. This is made possible through comprehensive integration of the key building blocks into monolithic integrated circuits founded on SiGe technology. The performance generated from the 22-44Gb/s PRBS Source is world class with the typical EYE having 400 fs rms jitter, 500 mV of output swing and <7 ps rise time.

All of this comes in a package one sixth the size of any other solution on the market which allows you to put your source directly at your device under test regardless of your lab bench environment.

Application

The Centellax 22-44Gb/s PRBS Source is designed to be used as the source for testing ultra-high speed communications components such as those used in OC 768 / STM 256 applications. The 22-44Gb/s PRBS Source is a perfect companion to a Digital Communication Analyzer in a stimulus response measurement for 40 Gb/s components such as driver amplifiers, transimpedance amplifiers, optical modulators, and DEMUX. Other applications include backplane signal integrity testing, and cable testing.

For 56G testing, the TG1P4A OPT112 includes an internal reference clock operating at 28.000Gbps.

Note: Outputs are CML and must be externally DC terminated with 50Ω to GND. One way to achieve DC termination while AC coupling is to use a Bias-Tee with its DC pin grounded through 50Ω.

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TG1P4A Datasheet

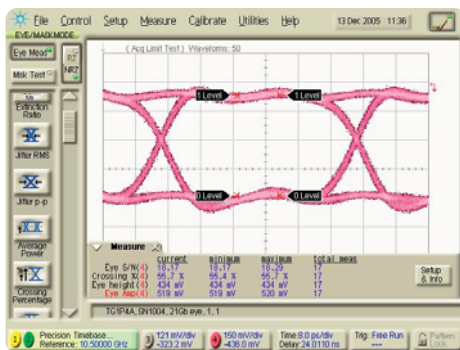


FRONT OF TG1P4A

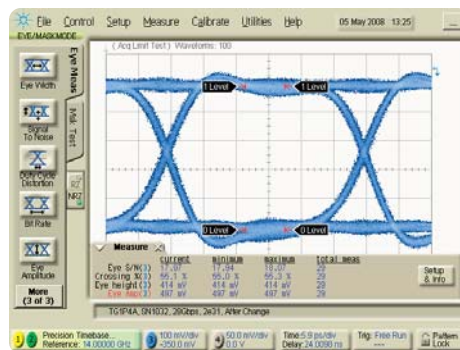


BACK OF TG1P4A

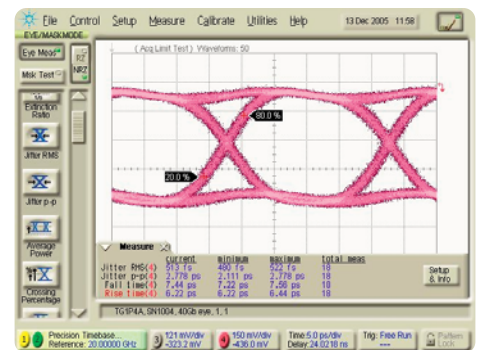
Showing the pattern control switches, clock inputs and outputs, and trigger outputs.



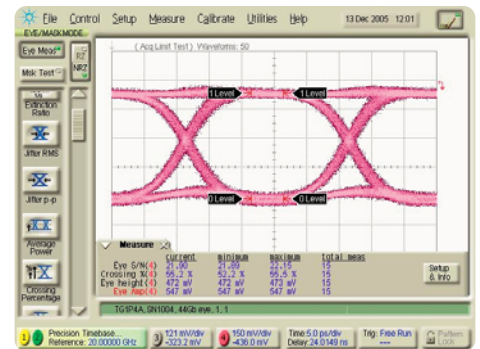
22 Gb/s



28 Gb/s



40 Gb/s



44 Gb/s

Label	Description	Connector Type
Power	Power Switch on/off	
Clk Input	External Clock Input (11 - 22GHz)	K
Clk Output	Internal Clock Output (19.9 GHz)	K
Clk / 1	'Clk Input' Output	K
Reset	Reset / PRBS Pattern	
Pattern Trigger	Pattern Trigger Output	SMA
Pattern Length	Pattern Selector	
	Logic	Pattern
	1 1	$2^{31} - 1$
	1 0	$2^{15} - 1$
	Polynomial Description	
		$1 + x^{28} + x^{31}$
		$1 + x^{14} + x^{15}$
		$1 + x^4 + x^7$

Options

- OPT003 Broadband Operating Range 22-44Gb/s
- OPT112 Internal Reference Clock Operation at 28.000 Gb/s
- OPT113 Internal Reference Clock Operation at 25.000 Gb/s

Performance Specification Table

	Description	Minimum	Typical	Maximum	Unit	
DATA OUTPUT	Bit Rate	TG1P4A 37	-	44	Gb/s	
		TG1P4A-OPT003 22	-	44	Gb/s	
	RMS Jitter	TG1P4A -	400	600	fs	
		TG1P4A-OPT003 -	400	1000	fs	
	Rise/Fall Times (20-80%)		6	8	ps	
	Amplitude		450	500	mVpp	
	SNR		-	18	-	
CLOCK OUTPUT	Offset		0	-	V	
	RMS Jitter		175	250	fs	
	Amplitude		2.8	4	Vpp	
	Frequency		-	19.9	GHz	
	CLOCK INPUT	Input Level		13	16	dBm
		Offset		0	-	V
		Frequency		11	22	GHz
PATTERN TRIGGER OUTPUT	Output Level		800	-	mV	
	Jitter		20	-	ps	
CLK/1 OUTPUT	Output Level		1	4	dBm	
PHASE ADJUSTMENT	Phase adjustment range		30	-	ps	
PATTERN TRIGGER	Pulse Period:	$64 * (1/\text{Output_Bit_Rate}) * (2^n - 1)$				
	Pulse Width:	$64 * (1/\text{Output_Bit_Rate})$				