

10 Gbps PRBS Source with Integrated Clock Test Accessory

Operating Manual



TG2P1A

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Printed in USA. 13 Jun 2008

smd-00057 rev A.

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Note: This product contains no user or factory adjustments. There is no calibration cycle or certificate.

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10G PRBS Source with Integrated Clock Test Accessory

TG2P1A Operating Manual

Section 1: Introduction

This manual is designed to familiarize users with the operation of the Centellax TG2P1A PRBS Source w/ Integrated Clock.

Section 2: Description

The Centellax TG2P1A Source with Integrated Clock is a Pseudo Random Bit Stream (PRBS) generator with an integrated internal clock that can be factory set from 9.85 - 11.35GHz. The TG2P1A can also be user-configured to use a 0.05 - 12.5GHz clock signal from an external source.

The TG2P1A features low jitter, fast rise and fall times, and a clean eye pattern. The source provides five selectable pattern lengths and three selectable mark densities. The TG2P1A comes in an easy to use compact (3.5x3.5x1.0 inch) package.

The PRBS generator provides the "clean eye" needed to evaluate the performance of optical system components or complete systems, e.g. SONET/SDH, 10 Gb/s ethernet, XAUI, etc.

Features

- Single-Frequency Clock Source
- Wide Operating Range, up to 12.5Gb/s (external clock)
- RMS Jitter ~ 1.5 ps
- Fast Rise/Fall Times
- Small size: 3.5" x 3.5" x 1"
- Multiple Output Patterns: 2^7 , 2^{10} , 2^{15} , 2^{23} , 2^{31}
- Multiple Mark Ratios: 1/2, 1/4, 1/8
- Differential Outputs
- Works to 14G with 2^7 , 2^{15} , 2^{23} , 2^{31} patterns

External Configuration

To configure the TG2P1A for the desired patterns (P) or mark space densities (D) apply the appropriate jumper to the configuration connector on the back of the TG2P1A. In the example below we are setting the pattern to $2^{31} - 1$ and the mark space density to $1/2$.

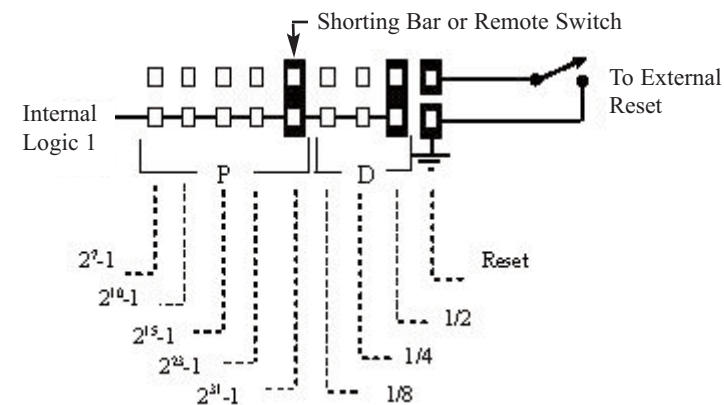


Figure 6: TG2P1A Configuration Connector

Physical Dimensions

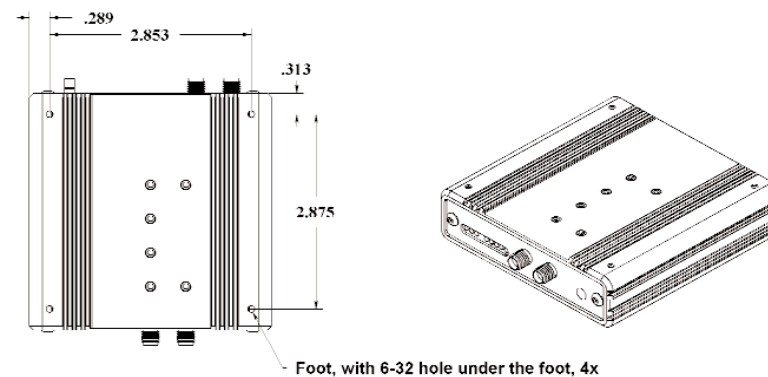


Figure 7: TG2P1A Dimensions

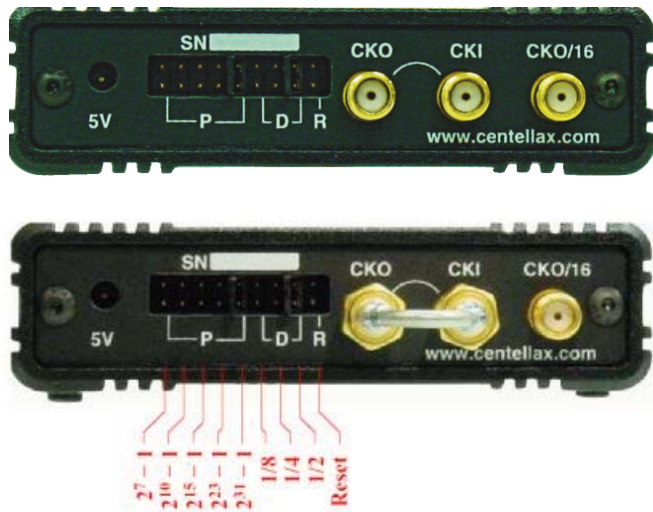


Figure 4: Rear panel of TG2P1A, top shows coax loop removed

Section 6: Application Example

A typical device measurement setup (using the internal clock) is shown in Figure 5. Additive jitter measurements require a precise, low jitter clock; a high-quality external clock source may decrease PRBS jitter.

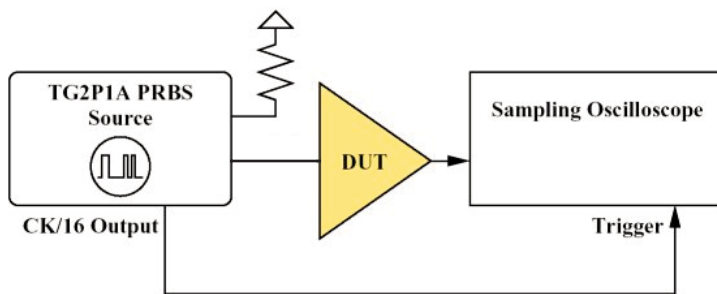


Figure 5: Typical measurement setup (referencing the internal clock)

Note: to maintain the integrity of the mm-wave system the user must select the appropriate connectors and minimize the length of microwave cabling. Contact Centellax for driver amplifiers, other application specific measurement accessories, and application support.

Section 3: Specifications

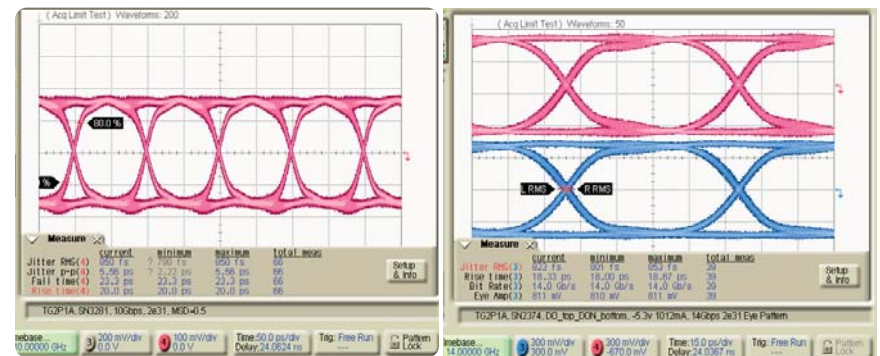
Table 1: Performance Specification

Description	Minimum	Typical	Maximum
TG2P1A PRBS Source			
Int. Clock Speed	—	10.0GHz	—
Ext. Clock Speed	0.05 GHz	—	12.50 GHz
Output Bit Rate *	0.05 Gb/s	—	12.50 Gb/s
RMS Jitter (Data) **	—	0.9 ps	—
RMS Jitter (Int. Clock)	—	1.0 ps	—
20-80 Rise/Fall Times	—	23 ps	25 ps
Eye Height	200 mV _(p-p)	250 mV _(p-p)	—
Eye Amplitude	250 mV _(p-p)	300 mV _(p-p)	—
OPT008 Eye Amplitude	700 mV _(p-p)	800 mV _(p-p)	—
Eye SNR ***	18	22	—
Output Voltage Low	—	-150 mV	—
Output Voltage High	—	+150mV	—
Clock Power	-1 dBm	+2 dBm	+3 dBm

* Min rate depends on input slew rate; lower rates are possible with fast input

** Measured with external clock and precision timebase

*** As measured with the Agilent 86100A DCA



10 Gb/s Eye Output from TG2P1A

14 Gb/s Eye Output from TG2P1A

TG2P1A Reset

The reset pin on the back panel can be used to reset the TG2P1A without using the front panel pushbutton switch. The new design of the TG2P1A has the pin below the "Reset" pin assigned to ground so that an external reset switch can be connected with a 2 pin connector (see Figure 6).

Table 2: Input Output Connectors

Connector	Description	DC Level	DC Level	Z0	Notes
Data+	Data Positive Output	0V	250mV	50ohm	DC blocked, ESD sensitive. SMA connector
Data-	Data Negative Output	0V	250mV	50ohm	DC blocked. ESD sensitive SMA connector
CKO	10G Clock Output	0V	>600mV	50ohm	DC blocked SMA Connector
CKI	External clock input	-5V to +5V max	>200mV	50ohm	DC blocked SMA connector
CKO/16	Clock divided by 16 output	0V	>300mV	50ohm	DC blocked SMA connector
P1-P5	Pattern Select	NA	NA	NA	Selected by closure to lower Pin - see figure 6
M1 - M3	Mark/space Select	NA	NA	NA	Selected by closure to lower Pin - see figure 6
Reset	Reset PRBS	NA	NA	NA	Selected by closure to lower Pin - see figure 6

Rear Panel

Rear Connector: Eight pins are provided to select the pattern length and mark density. A separate pin is provided to allow remote reset. Two jumpers are used to select the desired pattern length and mark density. Install the jumpers in the desired positions as shown in the figure below for stand alone operation. A cable can be connected to the pins for remote operation. See Figure 6.

CKO Output: A female SMA connector is provided for the internal clock output. The clock is factory-set and cannot be adjusted.

Impedance: 50ohms
 MaxDC: +/- 5V
 NominalDC: 0V
 AC Output: 600mV
 Note: ESD sensitive; terminate if unused
 DC blocked

CKI Input: A female SMA connector is provided for the PRBS clock input, which establishes the timing of the PRBS. A rigid coax loop is supplied to connect the CKO output to the CKI input; supply an external clock signal to the CKI input after removing the coax loop.

Impedance: 50ohms
 MaxDC: +/- 5V
 NominalDC: 0V
 AC Input: 200mV
 Note: ESD Sensitive; terminate if unused
 DC Blocked

CKO/16 Output: A female SMA connector is provided for a divided-by-16 clock input (CKO/16 = CKI div 16) for triggering.

Impedance: 50ohms
 MaxDC: +/- 5V
 NominalDC: 0V
 AC Onput: 600mV
 Note: DC Blocked

Power in: Negative 5 Vdc @ 1A (center pin negative) is supplied, by the power supply module, to this terminal to power the PRBS source.

Front panel

Reset Switch: A momentary reset switch provides a means to restart the bit stream from an all zero condition.

Output: The PRBS signal is available as a differential signal on the SMA female output terminals. Terminate unused outputs.

- Impedance: 50ohms
- MaxDC: +/- 5V
- NominalDC: 0V
- AC Level: 250mV
- Note: ESD sensitive; terminate if unused.
DC Blocked.

LED indicators: Eight LED annunciators are provided on the front panel. The first five indicate the selected pattern length. The next three indicate the selected mark density as illustrated below.



Figure 3: Front panel of TG2P1A

Section 4: Performance Verification

The figure below shows a configuration used to verify the performance of the PRBS source with an external clock. The TG2P1A internal clock can also be used, with the CLK/16 output triggering the sampling oscilloscope as illustrated in Figure 5.

This verification confirms the operation of five pattern lengths, mark density, and waveshape characteristics.

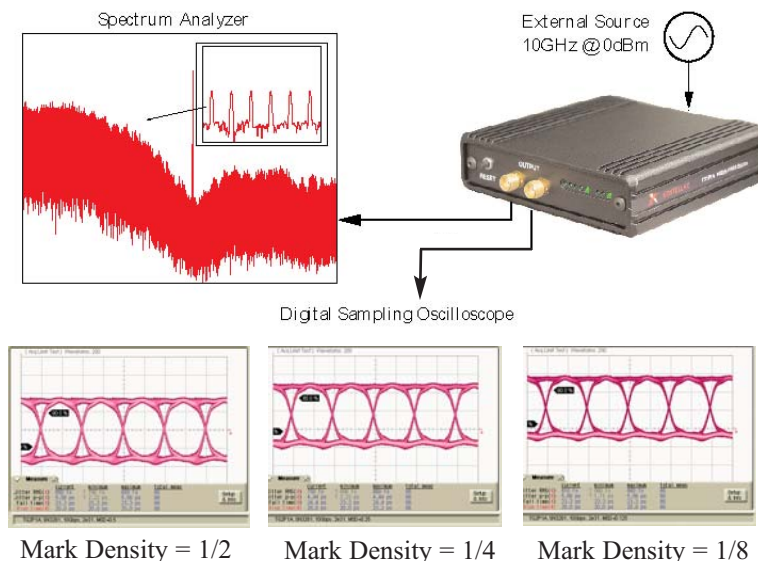


Figure 2: Verification Set-up

Correct pattern length is determined by confirming that the tone spacing on the spectrum analyzer equals $(\text{Output_Bit_Rate}/(2^n - 1))$, where n is the specific pattern length.

As an example, at 10 Gb/s the tone spacing for a $(2^{31} - 1)$ pattern should be ~ 4.66 Hz. (See table 3 for tone spacings)

Mark density is a measure of the number of logic 1's vs. total logic 1's and logic 0's. Standard PRBS patterns consist of equal numbers of 1's and 0's resulting in a mark density of 1/2.

The density of logic 1's and 0's can be qualitatively confirmed using a high speed sampling scope. A mark density of 1/2 will result in an output eye centered about 0 V. A mark density of 1/4 will result in an eye with a DC offset approximately equal to $(V_{pp}/2 - V_{pp} * MD)$ where MD is the mark density of 1/2, 1/4 or 1/8. Note that measurements made on the complimentary output will yield a similar DC offset but of opposite polarity.

Another method of qualitatively observing different mark densities is to observe the relative screen intensity for the two logic states. For MD = 1/2, the resulting eye will appear equally bright for logic 1's and 0's while an MD = 1/8 will yield a much brighter logic 0 vs. logic 1.

Waveform characteristics such as jitter, amplitude, rise and fall times are read directly from the sampling oscilloscope's measurements. Nominal measurements are all performed with a 0 dBm, 10 GHz input clock with a $(2^{31} - 1)$ pattern and mark density set to 1/2.

Support for verification set-up and DCA set-up procedures is available from Centellax.

Table 3: TG2P1A Pattern Properties

Pattern Length	Polynomial	Tone Spacing @ 10 Gb/s	ITU STD
$2^7 - 1$	$1 + X^6 + X^7$	78.7 MHz	ITU-T V.29
$2^{10} - 1$	$1 + X^7 + X^{10}$	9.78 MHz	CCITT O.1S2/ITU-T O.192
$2^{15} - 1$	$1 + X^{14} + X^{15}$	305 kHz	CCITT O.1S1/ITU-T O.151
$2^{23} - 1$	$1 + X^{18} + X^{23}$	1.19 kHz	CCITT O.1S1/ITU-T O.151
$2^{31} - 1$	$1 + X^{28} + X^{31}$	4.67 Hz	

Section 5: Operation

The TG2P1A Source w/ Integrated Clock provides a Pseudo Random Bit Stream (PRBS) referenced to either the factory-set internal clock (with frequencies from 9.85GHz to 11.35GHz) or the optional external clock (0.05GHz to 12.5GHz). Referencing either the internal or external clock, the TG2P1A generates a bit stream equal to the clock frequency, eg: 9.95328GHz = 9.95328Gb/s (SONET 10G).

The PRBS pattern length and mark density features can be selected by the user, as shown on page 10 & 11. The pattern length and mark density settings are indicated on the front panel of the TG2P1A.

When the TG2P1A is used in conjunction with a Digital Communications Analyzer, accurate high resolution measurements of optical components or systems can be performed. This source can also be used to generate the dithering sequences for high speed DAC's and ADC's.

For R&D applications the TG2P1A PRBS source provides the engineer with a fast rise/fall time, low jitter data stream which is useful in the development of optical products. Accurate repeatable eye pattern measurements provide a valuable development tool for evaluating and comparing the performance of design, or components.

The ultra small size of the TG2P1A (3.5x3.5x1.0 inch) allows close placement to DUT eliminating losses and distortion from long cables. The TG2P1A factory-set internal clock can be used to eliminate the need for additional test equipment clock signal generator or oscilloscope trigger divider).

In the manufacturing environment, the TG2P1A source provides a cost effective solution for evaluating and tuning communication systems such as SONET/SDH, 10 Gb/s Ethernet, fiber channel, XAUI, etc.